AMENDMENTS TO THE CLAIMS

1. (Currently amended) A communication parallel processing system comprising:

an input bus;

N task orientated processing devices, wherein N is greater than 1 and each of the task-oriented devices ~~providing~~ provides a particular function;

M buffers connected to said input bus, wherein M is greater than 1, each one adaptable to operate in a plurality of different phases operatively coupled to the N task orientated processing devices, said phases including a Fast Write Phase, a Slow Read Phase, a Slow Write Phase and a Fast Read Phase; and

a Time Division Multiplex Control mechanism operatively connected to the M buffers and imposing respective ones of the different phases on said M buffers to deliver outputs from said buffers to an output bus in the order that inputs were outputted on the said input bus; wherein said each one of the M buffers further includes a slow write port receiving data if said each one of the M buffers is in the Slow Write Phase, a slow read port providing data if said each one of the M buffers is in the Slow Read Phase, a fast write port receiving data if said each one of the M buffers is in a Fast Write Phase and a Fast Read Phase providing data if said each one of the M buffers is in a Fast Read Phase.

2. (Original) The parallel processing system of Claim 1 wherein M = N.

3. (Original) The parallel processing system of Claims 1 or 2 wherein the particular function includes cryptography

4 – 7 (Canceled)

8. (Currently amended) The parallel processing system of Claim ~~7~~ 19 wherein the TDM address generator includes a binary counter;

an address bus operatively coupled to the binary counter;

a decoder operatively coupled to the address bus; an inverter operatively coupled to the decoder;

an OR gate having a first input coupled to the inverter and a second input coupled to a Reset signal;

and an AND gate having a first input coupled to the OR gate, a second input coupled to a clock line and an output coupled to the binary counter.

9. (Currently amended) The parallel processing system of Claim ~~7~~ 19 wherein the TDM control circuit arrangement includes

a time base free running counter;

a TDM Reset Decoder operatively coupled to the output of the time base, free running counter;

a circuit arrangement that monitors space available in each of the M buffers and outputs a control pulse if the available space is less than the space required to store a predetermined size data block;

a delay line; and

a buffer counter operatively coupled to the delay line and the circuit arrangement.

10-14 (Canceled)

15. (Original) The parallel processing system of Claim 9 wherein the predetermined size data block includes a data frame or data packet.

16. (Original) The parallel processing system of Claim 15 wherein the space monitoring circuit arrangement includes a boundary MUX having an input from the buffer counter and a plurality of inputs of boundary signals one from each buffer indicating address reached in each buffer at end of fast write phase;

a subtractor responsive to output signal from the boundary MUX and output signal from the time base counter; and

a comparator responsive to an output signal from said subtractor and a signal indicating length of the data frame.

17- 18 (Canceled)

19. (New) A communication parallel processing system comprising:

an input bus;

N task orientated processing devices, wherein N is greater than 1 with each of the task-oriented devices providing a particular function;

M buffers connected to said input bus, M greater than 1, each one adaptable to operate in a plurality of different phases operatively coupled to the N task orientated processing devices;

a Time Division Multiplex Control mechanism operatively connected to the M buffers and imposing respective ones of the different phases on said M buffers to deliver outputs from said buffers to an output bus in the order that inputs were outputted on the said input bus; said Time Division Multiplex mechanism including one TDM slow read address generator operatively coupled to at least one of the M buffers, one TDM Slow Write address generator operatively coupled to the at least one of the M buffers, one TDM Fast Read address generator operatively coupled to the at least one of the M buffers, and at least one TDM fast write address generator operatively coupled to said at least one of the M buffers; and

a TDM Control circuit arrangement generating an output MUX control signal that drives said output multiplexor, a TDM Read Reset signal that drives the TDM slow read address generator and the at least one TDM Fast read address generator and a TDM write reset signal that drives the TDM fast write address generator and the TDM slow write address generator.